Amendments to the Claims

Claim 1 (currently amended):

A Turbo Codes Decoder is used as a baseband processor subsystem for iterative decoding a plurality of sequences of received data R_n representative of coded data X_n generated by a Turbo Codes Encoder from a source of original data u_n into decoded data x_n comprising of:

(a) two pipelined SISO Log-MAP Decoders each decoding input data from the other output data in an iterative mode.

(b) the first SISO Log-MAP Decoder having three inputs: R_0, R_1 connecting from ~~the~~ an Input shift register ~~module~~ buffer, and Z_1 feeding-back from the De-Interleaver Memory ~~module~~ output; and the first Decoder output is connected to an Interleaver Memory ~~module~~.

(c) the second SISO Log-MAP Decoder having two inputs: R_2 connecting from the Input shift register ~~module~~ buffer, and Z_2 connecting from the Interleaver Memory ~~module~~ output; and the second Decoder output is connected to a De-Interleaver ~~RAM~~ Memory.

(d) an Interleaver Memory ~~module~~ storing decoded data from the first Log-MAP Decoder, feeding data to the second Log-MAP Decoder.

(e) a De-Interleaver Memory ~~module~~ storing decoded data from the second Log-MAP Decoder, feeding-back data to the first Log-MAP Decoder.

(f) an Input Shift Register Buffer storing a block of input un-decoded received data, and feeding data to the two Log-MAP Decoders.

(g) a Control logic state machine controlling ~~the~~ overall operations of the Turbo Codes Decoder.

(h) a hard-decoder logic producing a final decision of either logic zero 0 or logic one 1 at the end of the iterations.

Claim 2 (currently amended):

The Decoder system of claim c1, wherein each Log-MAP decoder uses the logarithmic maximum a posteriori ~~probability~~ algorithm.

Claim 3 (currently amended):

The Decoder system of claim c1, wherein each Log-MAP decoder uses the soft-input and soft-output (SISO) logarithmic maximum a posteriori ~~probability~~ algorithm.

Claim 4 (currently amended):

The Decoder system of claim c1, wherein the Interleaver Memory ~~module~~ uses an ~~permuter~~ interleaver to generate ~~the~~ a write-address sequences of the Memory ~~core~~ in write-mode. In read-mode, the memory ~~core~~ read-address are normal sequences.

Claim 5 (currently amended):

The Decoder system of claim c1, wherein the Interleaver Memory ~~module~~ uses dual-port ~~memory~~ RAM.

Claim 6 (original):

The Decoder system of claim c1, wherein the De-Interleaver Memory module uses ~~an inverse-permuter~~ a de-interleaver to generate the write-address sequences of the Memory ~~core~~ in write-mode. In read-mode, the memory ~~core~~ read-address are normal sequences.

Claim 7 (original):

The Decoder system of claim c1, wherein the De-Interleaver Memory ~~module~~ uses dual-port ~~memory~~ RAM.

Claim 8 (cancelled):

Claim 9 (currently amended):

The Decoder system of claim c1, wherein ~~An 8-state~~ an n-state SISO Log-MAP Decoder for decoding a plurality of sequences of soft-input data SD_0 and SD_1 generated by a receiver to produce decoded soft-output data Y is comprising of:

(a) a Branch Metric module computing the two soft-input data SD_0 and SD_1 into ~~16~~ branch metric values for each branch in the ~~8-state~~ n-state trellis diagram.

(b) a Branch Metric Memory module storing the ~~16~~ branch metric values for each stage k = 0 ...N.

(c) a State Metric module computing forward and backward state metric values for each state in the trellis diagram using branch metric values.

(d) a State Metric Memory module storing ~~8-state~~ n-state metric values for each stage k = 0...N.

(e) a Log-MAP ~~module computing~~ computation module computing the ~~soft decision~~ output based on the branch metric values and state metric values using log maximum a posteriori probability algorithm.

(f) a Control Logic state machine module controlling ~~the~~ overall operations of the Log-MAP decoder

Claim 10 (cancelled):

Claim 11 (cancelled):

Claim 12 (cancelled):

Claim 13 (cancelled):

Claim 14 (cancelled):

Claim 15 (cancelled):

Claim 16 (cancelled):

Claim 17 (cancelled):

Title of the invention: HIGH SPEED TURBO CODES DECODER FOR 3G USING PIPELINED SISO LOG-MAP DECODERS ARCHITECTURE

Inventor Name: Quang Nguyen

Application Number: 09/681093

Signature:

Signature: Quang Nguyen Date: 7/16/03
Inventor Name: Quang Nguyen